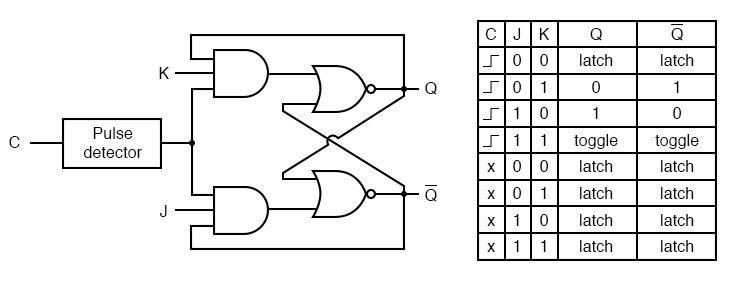
***Week 2.1 Problem Set: JK Flip-Flops***

Problem 1:

The ***JK Flip-Flop*** implements a toggle function when JK are both 1. Work with your instructor and breakout room to prove the state table below. For JK = 01 and 10, show Qn and !Qn result from both starting states (Qn-1 = 0 and !Qn-1 = 1 plus the opposite). For JK = 00 and 11, choose any one starting state.

*No need to hand anything in for this problem set, but take notes!*





*Whitespace left for your convenience*

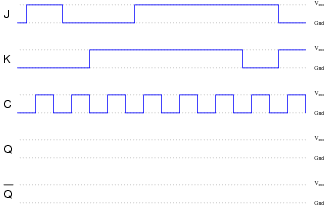
Latch – stays the same

Toggle – changes to the opposite state

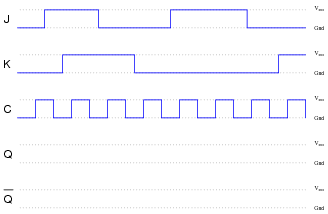
Problem 2:

Work through these two timing diagrams with your instructor and breakout room.



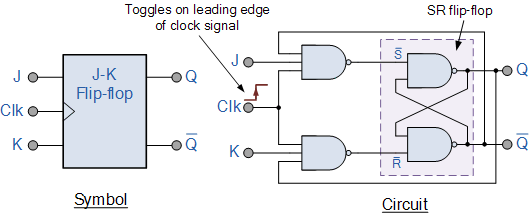






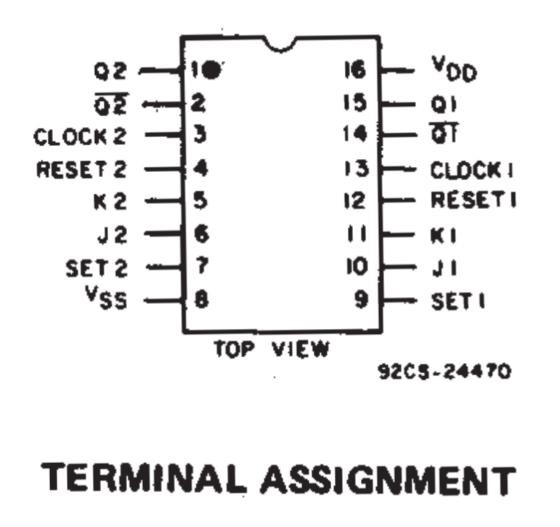
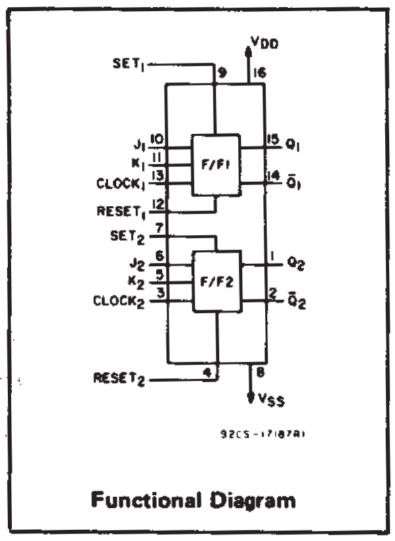


Problem 3:

The **CD4027BE** is the CMOS Dual JK Master-Slave Flip-Flop – look at its pinout and consider the uses of the Set and Reset inputs.



Asynchronous input with same function as JK except it doesn’t base it off a timer (preset flipflop before it begins ex. Hardwire 0,0)

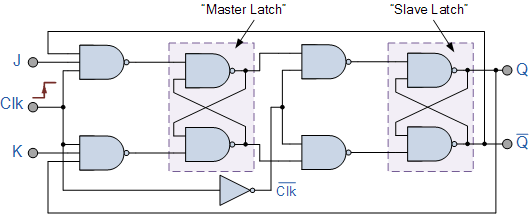


Problem 4:

***JK Flip-Flops*** can be configured in a ***master-slave*** configuration. Notice how the clock is wired up compared to a ***basic JK Flip-Flop (bottommost)***; how does this affect operation?

nbvcv

Edge triggered – when clock signal falls low and goes high, outputs are triggered



Tips:

* Good work starts with showing your work!
* Don’t be afraid to ask for help!
  + Consult your classmates and instructors if you get stuck.
  + Inform the instruction team if you have computer issues
* Credit to [allaboutcircuits.com/worksheets/flip-flop-circuits](https://www.allaboutcircuits.com/worksheets/flip-flop-circuits/) and [electronicstutorials.ws/sequential/seq\_2.html](https://www.electronics-tutorials.ws/sequential/seq_2.html)